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Design And Analysis of Sub-Harmonic PWM Techniques For A Nine Level Modular Multilevel Inverter

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ABSTRACT

The Modular multilevel inverter (M2LI) is one of the latest and most promising topology of multilevel inverters for high power applications. Several modulation strategies have been suggested for this topology. The objective of this paper is to design and investigate a suitable control technique for the prescribed topology, based on various sub-harmonic Pulse Width Modulation (PWM) techniques. The design involves selection of various parameters of the power circuit such as inductance and capacitance of the arm and sub-modules. Simulations have been performed for the PWM strategies in MATLAB and the results are discussed and compared.

INTRODUCTION

The modular multilevel inverter(M2LI) is a voltage-source-inverter(VSI) which is based on the cascaded interconnection of half bridge switching sub-modules(SMs or cells).The M2LI finds its application in high-voltage super-grids, frequency converters for railway inter-ties, medium voltage drives, DC-DC and indirect AC-AC power conversion and photo voltaic (PV) applications[1].

In this paper, design and steady state analysis of the M2LI topology have been carried out. Various sub-harmonics PWM modulation techniques such as phase disposition (PD-PWM), phase opposition disposition (POD-PWM), alternative phase opposition disposition (APOD-PWM) and phase shifted (PS-PWM) with suitable gating pattern have been done for the proposed topology and the obtained results were compared.

The outline of the paper is as follows. Section II deals with M2LI operating principles and various terminologies involved. Section III deals with the capacitance and inductance selection for the proposed topology, Section IV provides analysis and investigation of various sub-harmonic PWM techniques with the simulation and the validation of the results of the proposed topology. Finally, conclusion is presented in Section V.

MATERIALS AND METHODS

MODULAR MULTILEVEL INVERTER (M2LI)

A. Operation

The M2LI consists of a series of half-bridge cells cascaded in series which forms the phase-legs of the converter. Each leg consists of an upper and a lower arm consisting of series connected SMs and an arm inductor. The inductor serves the purpose of limiting the short circuit current through the leg. As the cells are connected in series, the current through the arm flows through each of the cells and affects the voltage of the capacitor. The capacitor charges and discharges as the positive and negative current flows through it [2].

To understand the operation of the proposed M2LI, let us consider a single cell of modular multilevel converter as shown in Fig.1.Here when main switch, S_m is on and when auxiliary switch, S_c is off, the output voltage is zero. When S_m is off and S_c is on, the output voltage is $V_o = V_{dc}$. Table 1 shows the switching states of a cell.

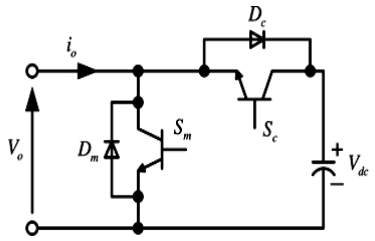


Fig.1 Structure of single cell of M2LI

TABLE I

SWITCHING STATE OF A SINGLE CELL

S_m	S_c	V_o	Current Direction	Power path	Capacitor state
On	Off	0	$i_o > 0$	S_m	Unchanged
On	Off	0	$i_o < 0$	D_m	Unchanged
Off	On	V_{dc}	$i_o > 0$	D_c	Unchanged
Off	On	V_{dc}	$i_o < 0$	S_c	Discharging

B. Nine level M2LI

By utilising the five level power circuit itself the nine-level output could be generated. It is achieved by means of employing a suitable sub-harmonic PWM technique.

For a five-level inverter as shown in Fig.2, there are (2n-2) capacitors and (n-1) cells in both upper and lower arm i.e. there are four capacitors and four cells in each arm. In the five-level modular inverter there are 70 switch states for each phase. These can be used collectively to generate a nine-level waveform in each phase of the inverter. The voltage levels $1/2V_{dc}$ and $-1/2V_{dc}$ can be obtained by switch combinations 11110000 and 00001111, respectively. These two switch states have no influence on the capacitor voltages. The voltage level $+1/4V_{dc}$ can be produced by 16 different switch combinations. For example, the switch state 01111000 charges C_1 and discharges C_6, C_7 and C_8 when $i_a > 0$; C_1 discharges and C_6, C_7 and C_8 charges when $i_a < 0$. The voltage level $-1/4V_{dc}$ is also produced by 16 different switch combinations. For example, the switch state 00010111 charges C_1, C_2, C_3 and discharges C_5 when $i_a > 0$, whereas it discharges C_1, C_2, C_3 and charges C_5 when $i_a < 0$. The zero voltage level can be generated by 36 different switch combinations. For example, when $i_a > 0$ the switch state 11000011 charges capacitors C_3, C_4 and discharges C_5, C_6; when $i_a < 0$ capacitors C_3, C_4 discharge and C_5, C_6 charges [3]. It is difficult to show all the 70 switch states hence the basic idea is as follows: Each sub-module consists of auxiliary switch and main switch. There are eight gating pulse patterns being obtained by comparing the triangular carriers with that of the sinusoidal reference. Each sub-module is given with the unique gating pulse with the condition that either the main switch or the auxiliary switch should be ON at any instance.

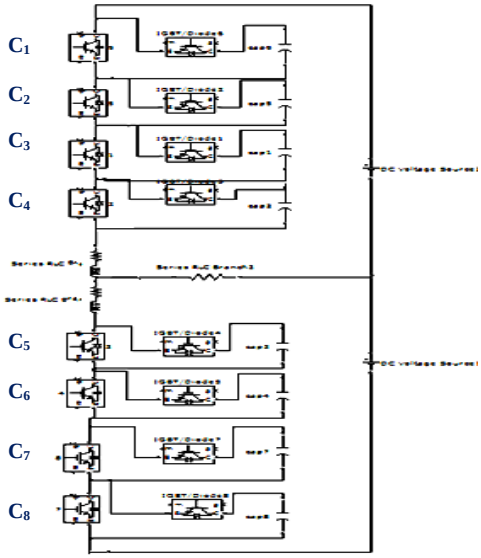


Fig.2. Power circuit of five-level M2LI

SELECTION OF CAPACITANCE AND INDUCTANCE

The capacitance and inductance selection is based on the circulating current and voltage ripple across sub-module capacitors. The selection of capacitance and inductance of M2LI is very essential as proper selection of such parameters drastically reduces the circulating current ac component, converter power losses and sub-module capacitor voltage ripples [4]. However, the circulating current ac component has a resonant character, which makes the analysis complex.
Now, the design of capacitance and inductance of the power circuit is as follows:

A. Capacitance Design

$EP = E_{cmax} / S_n$ (1)

Where

EP - Energy power ratio in J/KVA.

E_{cmax} - Maximum energy stored in capacitor in J.

S_n -Rated converter power in KVA

$E_{cmax}=8nC_{arm}V_{dc}^2/2n^2$ (2)

Where

8n – sub-modules where n=1.

C_{arm} – capacitances of the entire arm connected in series.

V_{dc} - voltage reference in upper or lower arm in volts,

$C_{arm}=E_{cmax}/4V_{dc}^2$ (3)

$C_{sm}=8C_{arm}$ (4)

Where

C_{sm} - sub-module capacitance in millifarads,

B. Inductance Design

$L_{arm}= [2(h^2-1) +m_a^2h^2]/ [\omega_rC_{arm}*8h^2(h^2-1)]$ (5)

Where

L_{arm}- arm inductance in millihenry,

h=2n, constant,

n=1, 2, 3…..∞,

m_a - modulation index, constant,

$\omega_r = 2\pi f_m$, angular frequency in rad/s.

f_m = 50Hz.

It is taken h=2n in order to eliminate second order harmonics because second order harmonics contribution to the circulating current is higher compared to other harmonics.

Based on the above design equations, the values of inductance and capacitance are obtained. The values of arm inductance and capacitance are 30 mH and 4.1666 mF, respectively. The value of 'h' is chosen as 10 because at this value a least Total Harmonic Distortion (THD) is obtained and the sub-module capacitance is assumed as 3.33 mF.

RESULT AND DISCUSSION

ANALYSIS OF SUB-HARMONIC PWM TECHNIQUES WITH SIMULATION RESULTS

The phase shifted and level shifted are the two most commonly employed sub-harmonic PWM schemes for multilevel inverters. The level shifted is again classified into three major types, they are in phase disposition (PD-PWM), phase opposition disposition (POD-PWM) and alternative phase opposition disposition (APOD-PWM) [5]-[8]. Let us consider all the above said modulation techniques as follows:

C. Phase shifted PWM (PS-PWM)

Phase-shifted multicarrier modulation is derived from unipolar modulation. The expression indicating the relation between the numbers of carriers and the number of voltage levels is shown in Eq. 6. All carriers must have the same frequency and peak-to-peak amplitude. Eq. 7 gives the phase difference between two carriers.

$$n_{carriers} = n_{voltage\ level} - 1 \quad (6)$$

$$\varphi_{carriers} = 360°/(n_{voltage\ level} - 1). \quad (7)$$

In Fig.3.a, the carrier waveforms and sinusoidal reference is illustrated. Fig.4.a. denotes the pulses and control signals for the switches of an arm with 8 modules. Fig.5.a. denotes the output voltage waveform obtained for a nine-level M2LI for RL load using phase shifted PWM.

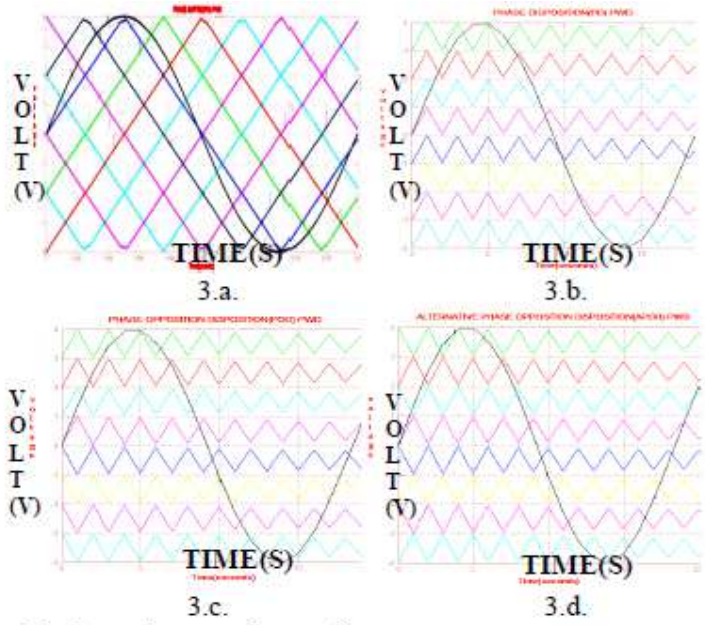


Fig.3. carrier waveforms of
3.a – phase shifted PWM; 3.b – phase disposition PWM.
3.c – phase opposition disposition PWM.
3.d – alternative phase opposition disposition PWM.

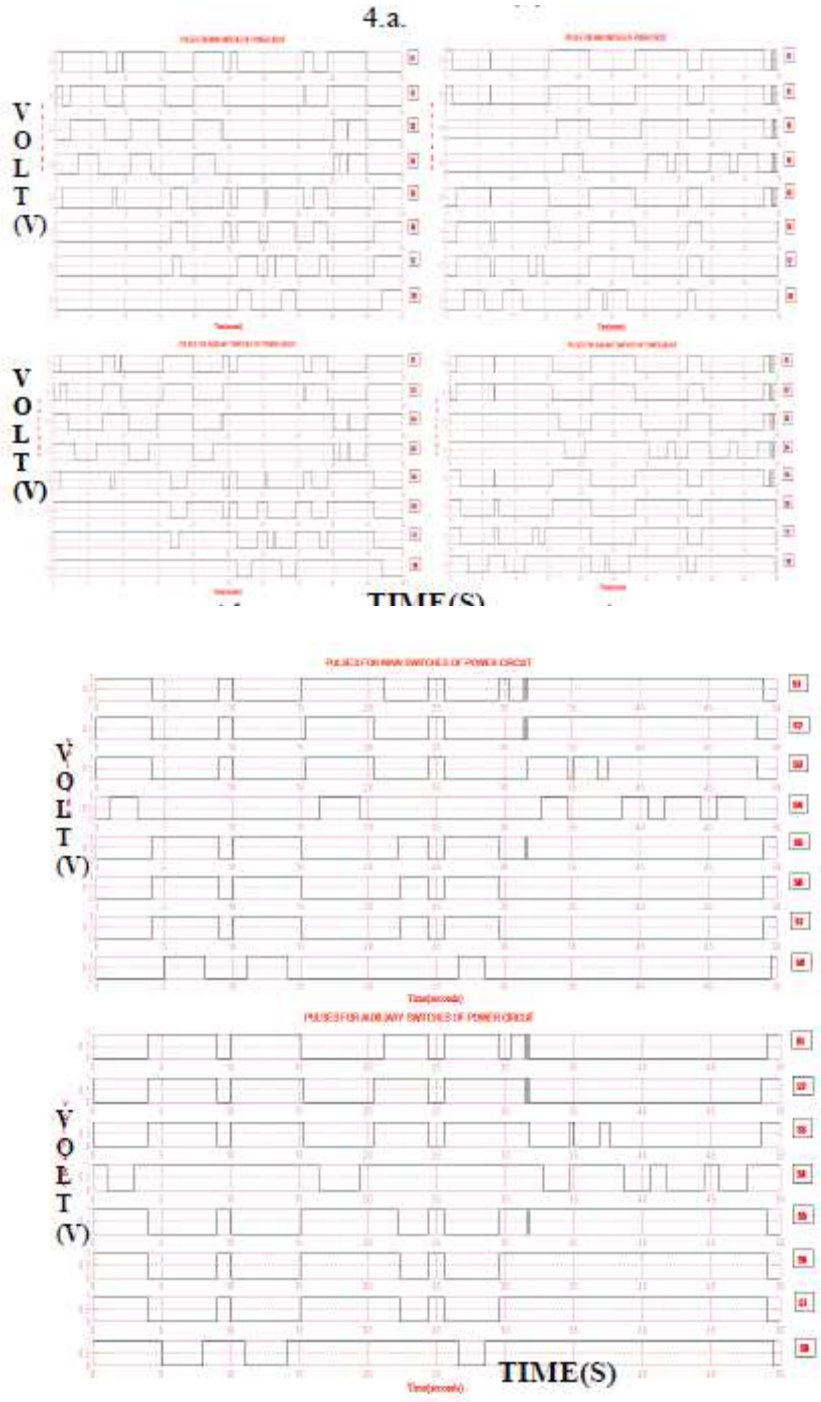


Fig.4.a. – phase shifted PWM.
4.b. – phase disposition PWM.
4.c. – phase opposition disposition PWM.
4.d. – alternative phase opposition disposition PWM.

gating pulses and control signals for the eight main switches followed by the eight auxiliary switches.

D. Phase disposition PWM(PD-PWM)

The in phase disposition, or PD, is based on a single carrier that is multiplied across the entire voltage range. The difference between any two carriers is shown only in the voltage offset, which represents the actual step size of the modulation. In Fig.3.b, the carrier waveforms and sinusoidal

reference is illustrated. Fig.4.b. denotes the pulses and control signals for the switches of an arm with 8 modules. Fig.5.b. denotes the output voltage waveform obtained for a nine-level M2LI for RL load using phase disposition PWM.

E. Phase opposition disposition PWM (POD-PWM)

The phase opposite disposition, or POD, uses two carriers, one for the positive voltage levels and one for the negative voltage levels. The negative voltage levels are shifted by 180 degrees with respect to the carrier for the positive voltage levels. The sign of their corresponding voltage levels in order to fill the entire voltage range then multiplies the carriers. In Fig.3.c, the carrier waveforms and sinusoidal reference is illustrated. Fig.4.c. denotes the pulses and control signals for the switches of an arm with 8 modules. Fig.5.c. denotes the output voltage waveform obtained for a nine-level M2LI for RL load using phase opposition disposition PWM.

F. Alternative phase opposition disposition PWM (APOD-PWM)

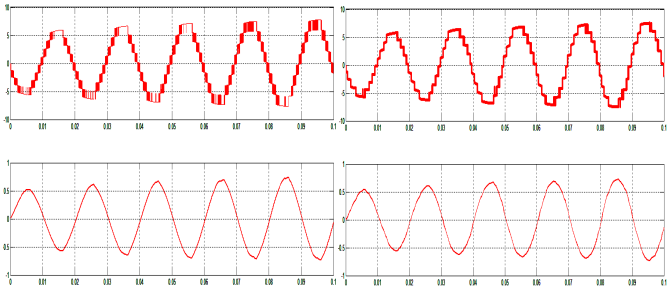
The alternative phase opposite disposition, or APOD, is based on two carriers that vary in the initial starting voltage level and phase. These two carriers are then multiplied over the entire voltage range. In Fig.3.d, the carrier waveforms and sinusoidal reference is illustrated. Fig.4.d. denotes the pulses and control signals for the switches of an arm with 8 modules.

Fig.5.d. denotes the output voltage waveform obtained for a nine-level M2LI for RL load using alternative phase opposition disposition PWM.

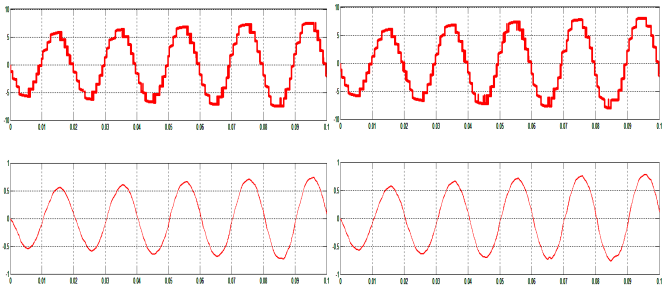
The Matlab/Simulink simulation have been carried out for the nine-level M2LI using all the four modulation techniques. Fig.5, represents the obtained output voltage and output current waveforms. Fig.6, represents the voltage THD, current THD versus ma, mf. It is clear from the Fig.6, phase shifted PWM (PS-PWM) technique has the least THD and balanced output voltage waveform. Table 2 represents the simulation parameters for the nine-level M2LI. It is clear from the Fig.6, for various m_f and m_a versus V-THD and I-THD, PS-PWM has the lowest THD and it is declared the best suited PWM technique for the modular inverter topology.

TABLE 2
SIMULATION PARAMETERS FOR NINE-LEVEL M2LI

Modulation index, m_a	1
frequency of modulation, m_f	99
Arm Inductance (L_{arm}) and arm resistance (R_{arm})	30mH, 0.1Ω
Load resistance, R_L	10Ω
Sub-module capacitance,C_{sm}	3.33mF
Voltage reference, V_{ref}	48 volts
Rated converter power, S_n	38.4 watts
Frequency, f_m	50 Hz



5.a. 5.b.



5.c. 5.d.

Fig.5. Output voltage and output current waveforms of nine-level modular multilevel inverter for RL load using

5.a - phase shifted PWM; 5.b.- phase disposition PWM.

5.c. - phase opposition disposition PWM.

5.d. – alternative phase opposition disposition PWM.

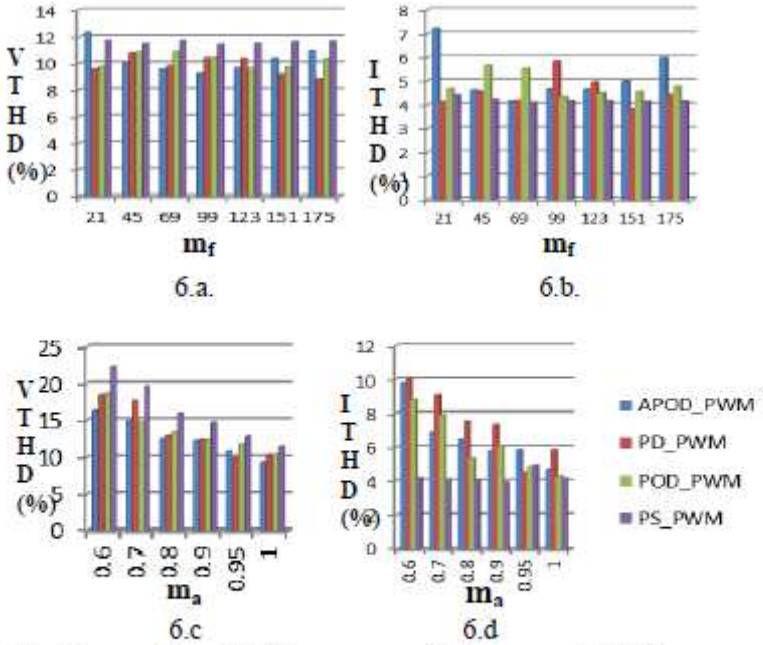


Fig.6.a – voltage THD versus m_f; 6.b – current THD versus m_f at constant $m_a = 1$ for all modulation techniques.

Fig.6.c – voltage THD versus m_a; 6.d – current THD versus m_a at constant $m_f = 99$ for all modulation techniques.

CONCLUSION

The operating principle, four different sub-harmonic PWM modulation strategies and selection of capacitance and inductance for the nine-level modular inverter have been discussed. Based on the results, it is found that phase shifted PWM compared to the other techniques has the balanced output voltage with the least THD. By using the above modulation technique, nine-level output is achieved with reduced number of switches compared to the conventional nine-level modular inverter. Therefore, PSPWM is the best suited PWM technique for the proposed modular inverter.

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